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| 09/994,574 | 11/26/2001 | William R. Wheeler | 10559/602001/P12886 | 7301 |

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| EXAMINER | |
|---|---|
| GUILL, RUSSELL L | |

| ART UNIT | PAPER NUMBER |
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| 2123 | |

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/994,574 | WHEELER ET AL. | |
| | Examiner | Art Unit | |
| | Russ Guill | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-7,9-13,15,18,20-23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9-13,15,18,20-23 and 25-27* is/are rejected.

7)☐ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This action is in response to an Amendment filed July 17, 2006. No claims were cancelled. Claims 26 - 27 were added. Claims 1, 3 - 7, 9 - 13, 15, 18, 20 - 23 and 25 - 27 are pending. Claims 1, 3 - 7, 9 - 13, 15, 18, 20 - 23 and 25 - 27 have been examined. Claims 1, 3 - 7, 9 - 13, 15, 18, 20 - 23 and 25 - 27 have been rejected.

2. The Examiner would like to thank the Applicant for the well-presented response, which was useful in the examination process. The Examiner appreciates the effort to perform a thorough analysis and make appropriate arguments and amendments.

3. This Office Action is NON-final due to relevant new art located during a search update.

### *Response to Arguments*

4. Regarding claims 1, 7, 15 and 18 rejected under 35 U.S.C. § 103:

   4.1. Applicants' arguments have been considered but are moot in view of the new ground(s) of rejection. An updated search yielded new relevant art.

### *Claim Objections*

5. Claim 7 is objected to for the following informalities: Claim 7 appears that it may have limitations 4 - 6 in reverse order.

### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims **1, 5 - 6, 26 - 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (U.S. Patent Application Publication 2002/0023250) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

**8.1.** The art of Yumoto is directed to logic design systems *(page 1, paragraph [0002])*.

**8.2.** The art of Yamagishi is directed to logic design systems *(page 13.2.1, Abstract, and section 1 Introduction)*.

**8.3.** Regarding **claim 1**:

**8.4.** Yumoto appears to teach:

**8.4.1.** a logic design module operable to be used by one or more users to generate a logic design as part of an electrical circuit, wherein the logic design includes labels *(figure 15, it would have been obvious that a logic design module was used to build the displayed code, wherein the logic design module was a tool such as SILOS III from Simucad; and page 2, paragraph [0029])*.

8.4.2. a collection of modifiable values of signal parameters that are accessible by the logic design module, wherein the values of signal parameters are associated with the labels in the logic design (*figure 14; and figure 15,it would have been obvious that the included file np1_param_define.v contained bit width signal parameters with labels cst1_packet_in_width and cst1_packet_out_width, and it would have been obvious that the signal parameters were accessible by the logic design module; and page 2, paragraph [0029]*).

8.4.3. The logic design module is operable to update the logic design to reflect modification of the values of the signal parameters by modifying the logic design to be compatible with the modified values of the signal parameters (*figure 15, it would have been obvious that compiling the Verilog code would have used the signal parameters in file np1_param_define.v to modify the signal widths to be compatible with the modified values of the signal parameters; and page 2, paragraph [0029]*).

8.5. Yumoto does not specifically teach:

8.5.1. *a central database integrated with the logic design module*.

8.5.2. The logic design module is operable to update the logic design to reflect modification of the signal parameters *in the central database*.

8.6. Yamagishi appears to teach:

8.6.1. a central database integrated with the logic design module (*pages 13.2.2 and 13.2.3, section 2.2 Database FALNET*).

8.7. Yumoto and Yamagishi are analogous art because they are both directed to the art of logic design systems.

8.8. The motivation to use the art of Yamagishi with the art of Yumoto would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks *(page 13.2.3, left-side of page, lines 1 - 3)*, and the expressed benefit in Yumoto of the software to save designers time and effort by simplifying the maintenance of the design *(page 2, second paragraph)*.

8.9. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi with the art of Yumoto to produce the claimed invention.

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8.10. Regarding claim 5:

8.11. Yumoto appears to teach:

8.11.1. the signal parameters characterize a signal bit width (*figure 15, input signal d, element cst1_packet_in_width*).

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8.12. Regarding claim 6:

8.13. Yumoto appears to teach:

8.13.1. the signal parameters characterize a signal bit position (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

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8.14. Regarding claim 26:

8.15. Yumoto appears to teach:

8.15.1. the signal parameters define characteristics that characterize multiple bits of a multiple bit signal (***figure 15, input signal d, element [cst1_packet_in_width-1:0]***).

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8.16. Regarding claim 27:

8.17. Yumoto appears to teach:

8.17.1. the signal parameter defines a characteristics that characterizes multiple bits of a multiple bit signal (***figure 15, input signal d, element [cst1_packet_in_width-1:0]***).

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9. Claims 3 - 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto as modified by Yamagishi as applied to claims 1, 5, 6, 26 - 27 above, further in view of IEEE Verilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

9.1. Yumoto as modified by Yamagishi teaches a logic design system as recited in claims 1, 5, 6, 26 - 27 above.

9.2. The art of IEEEVerilog is directed to logic design ***(page iii, section Introduction)***.

9.3. Regarding claim 3:

9.4. Yumoto does not specifically teach that the logic design module is structured and arranged to indicate design discrepancies automatically in the logic design resulting from the modifications to the values of the signal parameters in the central database.

9.5. Yamagishi appears to teach a central database integrated with the logic design module *(pages 13.2.2 and 13.2.3, section 2.2 Database FALNET).*

9.6. IEEEVerilog appears to teach indicating design discrepancies automatically in the logic design resulting from the modifications to the values of the signal parameters *(page 59, lines 1 - 25)*.

9.6.1. Regarding *(page 59, lines 1 - 25)*; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

9.7. Yumoto and IEEEVerilog are analogous art because they both include the problem of logic design.

9.8. The motivation to use the art of IEEEVerilog with the art of Yumoto as modified by Yamagishi would have been that indicating design discrepancies earlier in the design before generating Verilog computer code would save time and effort.

9.9. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of IEEEVerilog with the art of Yumoto as modified by Yamagishi to produce the claimed invention.

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9.10. Regarding claim 4:

9.11. Yumoto appears to teach indicating a bit width *(figure 15, input signal d has a bit width)*.

9.12. Yumoto does not specifically teach indicating a bit width *error*.

9.13. IEEEVerilog appears to teach indicating a bit width error *(page 59, lines 1 - 25)*.

9.13.1. Regarding *(page 59, lines 1 - 25)*; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

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10. Claims 7, 11 - 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (U.S. Patent Application Publication 2002/0023250) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

10.1. Regarding claim 7:

10.2. Yumoto appears to teach:

10.2.1. receiving an assignment of a value to a signal parameter *(figure 15; it would have been obvious that element cst1_packet_in_width received an assigned value)*

10.2.2. Maintaining the value of the signal parameter in association with an identifier of the signal parameter *(figure 14; it would have been obvious that the value of a signal parameter was maintained)*.

**10.2.3.** Using the identifier of the signal parameter to identify a first position in computer code for a logic design forming part of an electrical circuit *(figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would use the identifier of the signal parameter to identify all positions in the computer code where th eidentifier was used)*.

**10.2.4.** Modifying the computer code at the first position to reflect the value (*figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would modify the computer code at all positions to reflect the value*).

**10.2.5.** Using the identifier of the signal parameter to identify a second position in computer code for the logic design (*figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would use the identifier of the signal parameter to identify all positions in the computer code where the identifier was used)*.

**10.2.6.** Receiving an updated value of the signal parameter (*Abstract; and figure 14; and figure 15, element cst1_packet_in_width; and page 2, paragraph [0029]; it would have been obvious that an updated value of the signal parameter was received* ).

**10.2.7.** Modifying the computer code at the second position to reflect the value (*figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would modify the computer code at all positions to reflect the value*).

**10.2.8.** Updating both the first position and the second position in the computer code for the logic design to reflect the updated value of the signal parameter (*figure 15, element cst1_packet_in_width; it would have been obvious that when the code was compiled that the Verilog compiler would update all positions in the computer code for the logic design to reflect the updated value of the signal parameter*).

10.3. Yumoto does not specifically teach:

10.3.1. Maintaining the defined signal value *in a central database*.

10.3.2. Using the identifier of the signal parameter maintained *in the central database* .

10.3.3. Receiving an updated value of the signal parameter *in the central database*.

10.4. Yamagishi appears to teach a central database integrated with a logic design module *(pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)*.

10.5. The motivation to use the art of Yamagishi with the art of Yumoto would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks *(page 13.2.3, left-side of page, lines 1 - 3)*, and the expressed benefit in Yumoto of the software to save designers time and effort by simplifying the maintenance of the design *(page 2, second paragraph)*.

10.6. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi with the art of Yumoto to produce the claimed invention.

10.7. Regarding **claim 11**:

10.7.1. Yumoto appears to teach:

10.7.1.1. the signal parameter characterizes a signal bit width and the value includes a value for the signal bit width (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

10.8. Regarding **claim 12**:

10.8.1. Yumoto appears to teach:

**10.8.2.** the signal parameter characterizes a signal bit position and the value includes a value for the signal bit position (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

**10.9.** Regarding claim **13**:

**10.9.1.** Yumoto appears to teach:

**10.9.2.** the signal parameter characterizes a bit field and the value includes a value for the bit field (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

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**11.** Claims **9 - 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto as modified by Yamagishi as applied to claims 7, 11 - 13 above, further in view of IEEE Verilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

**11.1.** Yumoto as modified by Yamagishi teaches a logic design method as recited in claims 7, 11 - 13 above.

**11.2.** Regarding claim **9**:

**11.3.** Yumoto does not specifically teach automatically indicating design discrepancies in the logic design that result from updating the value of the defined signal parameter.

**11.4.** IEEEVerilog appears to teach indicating design discrepancies automatically in the logic design resulting from the modifications to the signal parameters (*page 59, lines 1 - 25*).

**11.4.1.** Regarding ***(page 59, lines 1 – 25)***; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

**11.5.** Yumoto and IEEEVerilog are analogous art because they both are directed to the problem of logic design.

**11.6.** The motivation to use the art of IEEEVerilog with the art of Yumoto as modified by Yamagishi would have been that indicating design discrepancies earlier in the design before generating Verilog computer code would save time and effort.

**11.7.** Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of IEEEVerilog with the art of Yumoto as modified by Yamagishi to produce the claimed invention.

**11.8.** Regarding **claim 10**:

**11.8.1.** Yumoto does not specifically teach:

**11.8.1.1.** graphically indicating a bit width error.

**11.8.2.** Yamagishi appears to teach graphically indicating bit widths (**figure 1**).

**11.8.3.** Yamagishi appears to teach graphically indicating errors (**figure 1**).

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**12.** Claim **15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (U.S. Patent Application Publication 2002/0023250) in view of Yamagishi (Yamagishi, Kunihiko; Sekine,

Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

12.1. Regarding claim 15:

12.2. Yumoto appears to teach:

12.2.1. a collection of identifiers of one or more bit width signal parameters (*figure 14*).

12.2.2. values associated with each of the identifiers of the bit width signal parameters (*figure 14*).

12.2.3. modification logic to allow a user to modify the values associated with the identifiers (*figure 14; it would have been obvious that a tool such as a text editor would allow the user to modify the values associated with the identifiers*).

12.2.4. an interface to convey the identifiers and the associated values to a logic design module that uses the identifiers to identify where a logic design is to be changed and the values to change a bit width in the logic design to form part of an electrical circuit (*figure 15, element cst1_packet_in_width; it would have been obvious that there was an interface, such as a Verilog compiler, between the include file npl_param_define.v and the code in order to identify where the logic design was to be changed*);

12.3. Yumoto does not specifically teach:

12.3.1. *A central database accessible by one or more users.*

12.3.2. One or more signal parameters defined *in the central database*.

12.3.3. an interface to convey the identifiers and the associated values from *the central database*.

12.4. Yamagishi appears to teach a central database accessible by one or more users *(page 13.2.1, figure 1, and pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)*.

12.5. Yumoto and Yamagishi are analogous art because they are both directed to the art of logic design systems.

12.6. The motivation to use the art of Yamagishi with the art of Yumoto would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks *(page 13.2.3, left-side of page, lines 1 - 3)*, and the expressed benefit in Yumoto of the software to save designers time and effort by simplifying the maintenance of the design *(page 2, second paragraph)*.

12.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi with the art of Yumoto to produce the claimed invention.

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13. Claims **18, 22, 23, 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (U.S. Patent Application Publication 2002/0023250) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

13.1. Regarding claim **18**:

13.2. Yumoto appears to teach:

13.2.1. Receiving a value of a signal parameter that characterizes multiple bits of a multiple bit signal *(figure 14, element GEN_WIDTH; it would have been obvious that a value was received in order to enter the value)*.

**13.2.2.** Maintaining the value of the signal parameter *(figure 14, element GEN_WIDTH)*.

**13.2.3.** Using the value of the signal parameter that is maintained, in computer code for a logic design forming part of an electrical circuit that includes the multiple bit signal *(figure 15, element cst1_packet_in_width)*.

**13.2.4.** Receiving an update to the value of the signal parameter (page 2, paragraph [0029]).

**13.2.5.** updating the logic design with the updated value of the signal parameter by modifying the logic design to be compatible with the updated signal parameter *(figure 15; it would have been obvious that compiling the Verilog code would have updated the logic design by modifying the logic design to be compatible with the updated signal parameter, since the parameter cst1_packet_in_width would be updated with a value from the include file np1_param_define.v)*.

**13.3.** Yumoto does not teach specifically teach:

**13.3.1.** Using the defined signal parameter *that is maintained in the central database* in computer code for a logic design forming part of an electrical circuit.

**13.3.2.** Maintaining the value of signal parameter *in a central database*.

**13.3.3.** Using the value of the signal parameter that is maintained *in the central database*.

**13.4.** Yamagishi appears to teach:

**13.4.1.** Maintaining logic design data *in a central database (page 13.2.1, section 2 FALcyber, and pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)*.

**13.5.** The motivation to use the art of Yamagishi with the art of Yumoto would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than

other commercially available frameworks *(page 13.2.3, left-side of page, lines 1 - 3)*, and the expressed benefit in Yumoto of the software to save designers time and effort by simplifying the maintenance of the design *(page 2, second paragraph)*.

**13.6.** Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi with the art of Yumoto to produce the claimed invention.

**13.7.** Regarding **claim 22**:

**13.7.1.** Yumoto appears to teach:

**13.7.1.1.** the signal parameter characterizes a signal bit width and the value includes a value for the signal bit width (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

**13.8.** Regarding **claim 23**:

**13.8.1.** Yumoto appears to teach:

**13.8.1.1.** the signal parameter characterizes a signal bit position and the value includes a value for the signal bit position (*figure 15, input signal d, element [cst1_packet_in_width-1:0]*).

**13.9.** Regarding **claim 25**:

**13.9.1.** Yamagishi appears to teach:

**13.9.1.1.** permitting one or more users to access the central database *(page 13.2.1, figure 1)*.

14. Claims 20 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto as modified by Yamagishi as applied to claims 18, 22, 23, 25 above, further in view of IEEE Verilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

14.1. Yumoto as modified by Yamagishi teaches a machine accessible medium as recited in claims 18, 22, 23, 25 above.

14.2. Regarding claim 20:

14.3. Yumoto does not specifically teach automatically indicating design discrepancies in the logic design that result from updating the value of the defined signal parameter.

14.4. IEEEVerilog appears to teach indicating design discrepancies automatically in the logic design resulting from the modifications to the signal parameters *(page 59, lines 1 - 25)*.

14.4.1. Regarding *(page 59, lines 1 - 25)*; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

14.5. Yumoto and IEEEVerilog are analogous art because they both are directed to the problem of logic design.

14.6. The motivation to use the art of IEEEVerilog with the art of Yumoto as modified by Yamagishi would have been that indicating design discrepancies earlier in the design before generating Verilog computer code would save time and effort.

14.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of IEEEVerilog with the art of Yumoto as modified by Yamagishi to produce the claimed invention.

14.8. Regarding **claim 21**:

14.8.1. Yumoto does not specifically teach:

14.8.1.1. graphically indicating a bit width error.

14.8.2. Yamagishi appears to teach graphically indicating bit widths (**figure 1**).

14.9. Yamagishi appears to teach graphically indicating errors (**figure 1**).

15. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

*Conclusion*

16. The following reference is pertinent to the Applicant's disclosure, and teaches knoeldge of the ordinary artisan at the time of invention:

    16.1. Samier Palnitkar, "Verilog HDL A Guide to Digital Design and Synthesis", 1996, SunSoft Press; teaches a logic design module Silos III.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.
18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.
19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG